AMENDMENTS TO THE CLAIMS

Please amend claim 15-19, as follows.

1-14. (Cancelled)

15. (Currently Amended) A method for processing data received in a port of a switch ~~in port slice based on wide cell encoding and an external flow control command~~, the method comprising:

managing 64-bit entries in a receive synch FIFO;

receiving two chunks of 32-bit data from the receive synch FIFO;

detecting a ~~K0~~ special character in a first byte of at least one of the received two chunks of 32-bit data; and

extracting a destination slot from a state field in a cell header of the at least one chunk of 32-bit data when ~~K0~~ the special character is detected in the at least one chunk of 32-bit data.

16. (Currently Amended) The method of claim 15, further comprising:

determining whether the cell header is low-aligned or high-aligned or both;

writing 64-bit data to a data FIFO corresponding to the destination slot when the cell header is either low-aligned or high-aligned;

writing two 64-bit data to two data FIFOs corresponding to ~~the~~ two destination slots when the cell header is low-aligned and high-aligned; and

filling one said chunk of 32-bit data with idle characters when a cell does not terminate at the 64-bit boundary and a subsequent cell is destined for a different slot.

17. (Currently Amended) The method of claim ~~16~~ 15, further

comprising:

performing an early terminate to a cell that inserts ~~K0~~ a special character and ABORT state information in the data when an error condition is detected.

18. (Currently Amended) The method of claim ~~16~~ 15, further comprising:

stopping requests to a FIFO read arbitrator after a current cell is completely read from a FIFO RAM when a flow control condition is detected.

19. (Currently Amended) The method of claim ~~16~~ 15, further comprising:

delivering 64-bit data to a SERDES synch FIFO module and transmitter when non-idle data is received from a FIFO read arbitrator;

injecting a first alignment sequence to be transmitted to the SERDES synch FIFO module and transmitter when the FIFO read arbitrator indicates that a plurality of FIFO RAMs are empty

injecting a second alignment sequence to be transmitted to the SERDES transmitter when a programmable timer expires and a previous cell has been completely transmitted; and

indicating to the FIFO read arbitrator to temporarily stop serving any requestor until a current pre-scheduled alignment sequence has been completely transmitted.